Remarks

Receipt is acknowledged of the Office Action mailed September 20, 2005. Applicant respectfully requests reconsideration of the present application in view of the foregoing amendment, and the remarks which follow. No new matter is added with the amendments, which are fully supported by the specification.

Claims 1 and 3 have been amended. Claim 2 has been canceled. Claims 1 and 3-9 are pending in the application.

Applicant thanks the Examiner for acknowledging the claim for foreign priority. In addition, Applicant thanks the Examiner for the indication that claims 3-9 are allowed.

Claim Rejections under 35 USC § 103

Claims 1 and 2 stand rejected under 35 U.S.C. §103(a) as being unpatentable over by Published U.S. Patent Application No. 2004/0093457 to Heap ("Heap") in view of U.S. Patent No. 6,405,286 to Gupta et al. ("Gupta"). Applicant submits that claim 2 has been canceled and as such the rejection with respect to claim 2 is moot. With respect to the rejection as applied against claim 1, Applicant respectfully traverses this rejection for at least the following reasons.

Independent claim 1 recites, *inter alia*, "wherein the nonvolatile ferroelectric memory programs a code for differently controlling a memory interleave operation *depending on an access latency time and a restore latency time which are set in a memory interleave region corresponding to lower address bits of row address bits.*" (emphasis added). As noted by the Examiner, Heap fails to disclose "the memory interleaving operation is controlled depending on an access latency time and a restore latency time which are set in a memory interleave region corresponding to lower address bits of row address bits." Office Action, dated September 20, 2005, at 3. Accordingly, the Examiner relies on the disclosure of Gupta to cure this deficiency in Heap. However, Applicant respectfully submits that Gupta fails to cure the deficiencies of Heap.

Gupta discloses assigning memory interleaving schemes to bank bits based on the classification of the bank bits using a memory interleaving scheme lookup table. In contrast, independent claim 1 recites programming a "code for differently controlling a memory interleave operation depending on an access latency time and a restore latency time." The programmed code controls the memory interleave operation and changes the address path of the signal chip FeRAM array. Gupta use of a memory interleaving scheme lookup table does not anticipate this recited feature of the present invention. Accordingly, Gupta fails to cure all of the deficiencies of Heap.

In sum, the combination of Heap and Gupta would not result in the interleave control device as recited in amended claim 1. Therefore, the combination does not render claim 1 obvious. For the foregoing reasons, Applicant respectfully submits that claim 1 is allowable over Heap in view of Gupta. Accordingly, Applicant respectfully requests withdrawal of the rejection of claim 1 under 35 U.S.C. § 103(a).

CONCLUSION

In view of the above amendment and remarks, applicant respectfully requests that all objections and rejections be withdrawn and that a notice of allowance be forthcoming. The Examiner is invited to contact the undersigned attorney for applicant at 202-912-2160 for any reason related to the advancement of this case.

Respectfully submitted,

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